AMENDMENTS TO THE CLAIMS

Please **CANCEL** claims 2, 3, 14, 15 and 23, without prejudice or disclaimer.

Please **AMEND** claims 1, 4-6, 13, 16-22 and 24-33, as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A method for manufacturing a wire contact structure ~~of a wire~~, comprising steps of:

forming a wire made of an aluminum-based material;

depositing ~~an insulating layer~~ a silicon nitride layer ~~covering~~ on the wire at a temperature between about 280° C and about 400° C to form an insulating layer;

forming ~~patterning the insulating layer to form~~ a contact hole extending though the insulating layer and exposing the wire; and

forming a conductive layer ~~made~~ formed of indium zinc oxide (IZO) and electrically connected to the wire through the contact hole .

2-3. (Cancelled)

4. (Currently Amended) The method of claim 3, wherein the step of depositing the silicon nitride layer is performed for about 5 minutes to about 40 minutes ~~the insulating layer is deposited for a period in the range of 5-40 minute~~.

5. (Currently Amended) The method of claim 1, wherein the contact hole ~~is more~~ has a size between about ~~than~~ 0.5 mm X 15 μm and ~~less than~~ 2 mm X 60 μm.

6. (Currently Amended) The method of claim 1, wherein ~~the~~ a contact resistance ~~of~~ between the aluminum-based material~~,~~ and the ~~indium zinc oxide~~ IZO is less than 10% of a wire resistance of the wire.

7. (Original) The method of claim 6, wherein the contact resistance is less than 0.15 $\mu\Omega cm^2$.

8–12. (Cancelled).

13. (Currently Amended) A method for manufacturing a thin film transistor array panel, comprising steps of:

forming a gate wire formed of an aluminum-based material, the gate wire including a gate pad ~~by depositing and patterning an aluminum-based material~~;

~~forming a gate insulating layer~~ depositing a silicon nitride layer over ~~covering~~ the gate wire at a temperature between about 280° C and about 400° C to form a gate insulating layer;

forming a semiconductor layer on the gate insulating layer;

forming a data wire on the semiconductor layer;

forming a contact hole extending through the gate insulating layer and exposing the gate pad ~~by patterning the gate insulating layer~~; ~~and~~

depositing an indium zinc oxide (IZO) layer on the gate insulating layer and the data

wire; and

patterning the IZO layer to form ~~forming~~ a conductive layer electrically connected to the ~~wire~~ gate pad ~~by depositing and patterning indium zinc oxide~~.

14-15. (Cancelled)

16. (Currently Amended) The method of claim 13, wherein the step of depositing the IZO layer comprises a step of ~~indium zinc oxide is formed by~~ sputtering a compound ~~target~~ including In_2O_3 and ZnO.

17. (Currently Amended) The method of claim 16, wherein ~~the~~ a content rate of Zn in ~~a~~ the compound ~~of In_2O_3 and ZnO~~ is between about 15% and about 20% ~~in the range of 15-20 at%~~.

18. (Currently Amended) The method of claim 13, wherein the step of patterning the IZO layer ~~forming a conductive layer further comprising the~~ comprises a step of~~:~~ forming a pixel electrode connected to the data wire ~~when forming the conductive layer~~.

19. (Currently Amended) A method for manufacturing a thin film transistor array panel ~~for a liquid crystal display~~, comprising steps of:

forming a gate wire formed of an aluminum-based material on a substrate, the gate wire comprising ~~including~~ a gate line, a gate electrode ~~connected to the gate line~~ and a gate pad ~~connected to the gate line, and made of aluminum-based material on an insulating substrate~~;

depositing a silicon nitride layer at a temperature between about 280° C and about 400° C to form a gate insulating layer;

forming a semiconductor layer on the gate insulating layer;

forming a data wire including a data line ~~intersecting the gate line~~, a source electrode ~~connected to the data line and adjacent to the gate electrode~~ and a drain electrode ~~opposite to the source electrode with respect to the gate electrode by depositing and patterning a conductive layer~~;

~~depositing~~ forming a passivation layer over the gate insulating layer and the data wire;

forming a contact hole extending through ~~patterning~~ the passivation layer ~~along with~~ and the gate insulating layer ~~to form a contact hole~~ and exposing the gate pad; ~~and~~

depositing an indium zinc oxide (IZO) layer over the passivation layer; and

patterning the IZO layer to form ~~forming~~ a redundant gate pad connected to the gate pad through the contact hole ~~by depositing and patterning IZO~~.

20. (Currently Amended) The method of claim 19, wherein the step of patterning the IZO layer ~~further comprising the~~ comprises a step of~~:~~ forming a pixel electrode ~~connected to the drain electrode when forming the redundant gate pad~~.

21. (Currently Amended) The method of claim 19, wherein the data wire further comprises a data pad ~~connected to the data line~~, and

the step of patterning the IZO layer comprises a step of forming a redundant data pad connected to the data pad ~~when forming the redundant gate pad~~.

22. (Currently Amended) The method of claim 19, wherein ~~the insulating layer and~~ the step of forming the passivation layer comprises a step of depositing a silicon nitride layer at a temperature between about 280° C and about 400° C ~~are deposited in a temperature range of 280-400 °C~~.

23. (Cancelled)

24. (Currently Amended) The method of claim 19, wherein the step of depositing the IZO layer comprises a step of ~~is formed by~~ sputtering ~~target~~ a compound including In_2O_3 and ZnO.

25. (Currently Amended) The method of claim 24, wherein ~~the~~ a content rate of Zn in ~~a~~ the compound ~~of In_2O_3 and ZnO~~ is between about 15% and about 20% ~~in the range of 15-20 at%~~.

26. (Currently Amended) The method of claim 19, wherein the data wire and the semiconductor layer are simultaneously ~~together formed by a photolithography process using~~ patterned by a photoresist pattern having portions with different thicknesses ~~depending on the positions~~.

27. (Currently Amended) The method of claim 26, wherein the photoresist pattern comprises ~~has~~ a first portion having a first thickness, a second portion having a second thickness ~~thicker larger~~ greater than the first thickness ~~portion~~, and a third portion having a third thickness

~~thinner~~ smaller than the first thickness.

28. (Currently Amended) The method of claim 27, wherein a mask used for forming the photoresist pattern has a first area having a first transmittance, a second area having a second transmittance smaller than the first transmittance, and a third ~~part~~ area having a third transmittance greater than the first transmittance~~, a transmittance of the third part is higher than the first part and the second part, a transmittance of the first part is higher than the second part~~.

29. (Currently Amended) The method of claim 28, wherein the first portion ~~and the second portion~~ of the photoresist pattern ~~are respectively~~ is aligned on a portion between the source electrode and the drain electrode, and the second portion of the photoresist pattern is aligned on the data wire.

30. (Currently Amended) The method of claim 29, wherein the first ~~part~~ area of the mask includes a partially transparent layer~~,~~ or a pattern reducing a transmittance ~~smaller than the resolution of the exposure used in the exposing step, to regulate the transmittance of the first part~~.

31. (Currently Amended) The method of claim 30, wherein the first thickness ~~of the first portion~~ is less than ~~the~~ a half of the second thickness ~~of the second portion~~.

32. (Currently Amended) The method of claim 31, further comprising a step of~~:~~ depositing an ohmic contact layer between the data wire and the semiconductor layer.

33. (Currently Amended) The method of claim 32, wherein the data wire, the ohmic contact layer, and the semiconductor layer are ~~formed in the same~~ patterned by a single photolithography process.

34 – 41. (Cancelled).